PIANO FORMATIVO NAZIONALE
DEL PERSONALE DELL'ISTITUTO NAZIONALE DI FISICA NUCLEARE

PFN 2016

VIVADO TRAINING

PROGRAMMA

Essentials of FPGA Design (1 giorno)
Build an effective FPGA design using synchronous design techniques, instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments, set basic XDC timing constraints, and use the Vivado® Design Suite to build, synthesize, implement, and download a design.

Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints (3 giorni)
This course offers detailed training on the Vivado™ software tool flow, Xilinx design constraints (XDC), and static timing analysis (STA). Learn to use good FPGA design practices and all FPGA resources to advantage. Learn to fully and appropriately constrain your design by using industry-standard XDC constraints. Learn how the the Vivado IDE design database is structured and learn to traverse the design. Create appropriate timing reports to perform full STA and how to appropriately synthesize your design.

Debugging Techniques Using the Vivado Logic Analyzer (1 giorno)
As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use Vivado® logic analyzer debug solution helps minimize the amount of time required for verification and debug. This one-day course will not only introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the Vivado debug tool can address advanced verification and debugging challenges.