Corso Nazionale sulla Progettazione digitale VLSI

========== Programma di massima ==========

IMEC description + mission:
Imec performs world-leading research in nanoelectronics. It leverages its scientific knowledge with the innovative power of its global partnerships in ICT, healthcare and energy, delivering industry-relevant technology solutions. In a unique high-tech environment, its international top talent is committed to providing the building blocks for a better life in a sustainable society.
Imec is headquartered in Leuven, Belgium, and has offices in Belgium, the Netherlands, Taiwan, US, China and Japan. Its staff of more than 1,750 people includes over 650 industrial residents and guest researchers. In 2008, imec's revenue (P&L) was 270 million euro.
Mission of training center:
The IMEC Training Center (ITC) provides training for the teaching staff of polytechnic schools and universities, and for engineers from industry, under the 'public' brand-name MTC – Microelectronics Training Center. The ITC provides training to IMEC staff and PhD students under the internal brand-name DELFI. In the area of FAB operations and Safety, the ITC is joining hands with other groups to maintain a qualification system.
The training covers technology and design for “More Moore” and for Morethan-Moore”, but also related fields, such a bio, physics, and even management related topics such as IP-protection.
Most of the training sessions are recorded using web-cast technology. The ITC maintains a knowledge sharing site providing all recorded session in an on-line library for internal access within IMEC. The same technology is used to provide a more limited service to the Flemish academia and to the general public, often within the framework of local or international projects.
The Micro-electronic Training Center (MTC) is a key platform for the collaboration of IMEC with Flemish universities and polytechnic schools, and is an extension of the activities that were started in 1982 within the INVOMEC initiative.
MTC organizes and supports the training and education in nano-electronics towards these universities and polytechnic schools. This is done through training programs for the teaching staff (including preparation of laboratory sessions and exercises), through delegating experts to lecture in the schools and through investments in infrastructure, facilities and services (mainly the provision of EDA tools and access to cheap

prototyping).
MTC extends these training facilities towards the broader public, within IMEC, but also towards the local and international industry and towards other target groups (Flemish secondary education, professional retraining, society).
MTC provides an efficient transfer of know-how of the expertise built up within IMEC for the training of Flemish students, towards the local industry via training projects but also to the international community by general or dedicated initiatives.
MTC applies modern multimedia techniques and expands its business model to provide real-time-streaming to industry.

Detailed program.

Day 1 - Lecture 1
CMOS Process Overview, 90 nm and beyond – 90 mins – Jan Wouters
This lecture gives an overview of state of the art (90 nm and beyond) MOS processes. The process flow is covered, as well as several process modules; issues that impact the electrical behavior are prioritized. Throughout the lecture it is shown that the on-going shrinking today is never "business as usual": continuously this industry must come up with new technological features. Understanding these is to some extend important when selecting a technology and when then doing the actual design.
- Moore's law and the ITRS roadmap
- STI (shallow trench isolation; as opposed to locos)
- Description of a sub 100 nm MOS transistor
1. Gate stack, including SiON, high-k, strain
2. Implants and short channel effect
- Silicides
- Copper damascene processing (as opposed to aluminum)
- Lithography, including NGL (next generation lithography)
- CMP (chemical mechanical polishing)

Day 1 - Lecture 2 + 3
Advanced sub-90nm Design flow and issues – 180 mins – Stephen O Loughlin
This lecture provides an overview of the digital implementation flow from netlist to gds. Each step in the flow is described in detail with an emphasis on the additional challenges facing designers at 90nm and below. In order to cover all of the topics in sufficient detail, this would likely need to be a two-part lecture. However, it may be possible to shorten it to one 90 minute lecture if only a few of the topics are desired in detail.
- Overview of Design Flow and EDA tools
- Libraries and Technology - Files and Formats, IP
- Design Planning
- Placement and Optimization
- Clock tree synthesis
- Routing

- Parasitic Extraction
- Static Timing Analysis (also SSTA and OCV)
- Multi-Mode Multi-Corner
- Signal Integrity Analysis (Crosstalk)
- Power Analysis
- ECOs, Design Verification, and Tapeout

Day 2 - Lecture 4
DFT for 90nm and beyond – 90 mins – Ilse Vos
'Design for Test' will give an (non-exhaustive) overview of which silicon tests are available to find specific manufacturing defects. Some defects only affect timing (and not functionality), requiring at-speed and higher-than-at-speed test, more so for 90nm and below. Depending on the 'product aim' and the used technology some tests are more suitable. Each test, however, has its own impact on design and tester time and therefore on turn-around time and project cost. Nevertheless, choosing the correct test approach is fundamental for rapid yield ramp up. This lecture provides you a first insight on test and its consequences.
- Testing & its cost
- Types of Testing
- HW vector Compression
- Power & test
- Diagnostics and the future?

Day 2 - Lecture 5
Low Power Digital Design : Implementation Perspective – 90 mins – Stephen O Loughlin
This lecture addresses the challenges faced by implementation engineers when creating designs that incorporate the latest low-power techniques. A review of the different strategies for power reduction is provided along with a description of several topics related to power analysis. The main focus then shifts to the implementation process, with an emphasis on the design and scheduling impact of the different low-power techniques.
- Review of techniques for dynamic and leakage power reduction
Clock-Gating
Logic Tuning
Multi-VT
Multi-Voltage
Power Gating
Substrate Biasing
- Power Analysis Topics
IR-drop
Electromigration
Static and Dynamic Analysis
Review of power analysis tools
- Low Power Implementation
CPF and UPF
Power Planning and Power Grid Design
Multi Voltage - Level Shifters
Power Gating - Isolation, State Retention, Power Switches

Power Aware Optimization

Day 2 - Lecture 6
Advanced Verification – 100 min – Jan-Willem Weijers
- Why verification is not business as usual.
- Simulation of power shut off / power up by means of CPF or UPF files.
- Automated coding rule checking (e.g. Spyglass).
- Assertion based simulation with links to PSL, SystemVerilog binding and formal verification.
- Random stimuli generation + coverage measurement.
- Open Verification Methodology (OVM).
- conformal analysis and verification

Day 3 - Lecture 7
Europractice – 120 mins – Carl Das, Paul Malisse, Steven Redant
This lecture will give an overview of the current services provided by Europractice, and an outlook of services and technologies to come. The lecture will highlight some special services for project that go beyond prototyping, and that need small volume, and yield, for detector experiments. Overview of best-practice procedures, and how and why to benefit from high-level experience in tape-out generation, test and assembly.
- Technology portfolio
1. UMC 90nm
2. TSMC 90nm, 65nm and 40nm
- PDK's and library overview, library characterisation
- Layout Services
1. Interfaces
2. Design flow
3. Digital on top
4. Analog on top
- Tape out procedures, checks (DRC, ERC, LVS) + DFM checks on 40nm
- Prototyping
- Assembly
- Test
1. HW and SW development
2. Tester selection
3. Prototype debug and characterisation
4. qualification
- Small Volume
1. Corners
2. Failure analysis
3. Yield optimisation
- Packaging portfolio and issues

Day 3 - Lecture 8
Radiation Tolerant Library – 45 minutes – Steven Redant
- What is DARE?
- Used hardening techniques

- Overview of available libraries & generators in the DARE family
- Comparison with commercial .18 library
- Backend services overview
- Legacy & current projects
- Radiation test results so far
- Status of 90 nm DARE work
- Currently running projects and future work
- How to get access

Day 3 - Lecture 9
3D Technology – Status and Roadmap – 120 mins – Nikolaos Minas
Over the last 4 decades, the semi-conductor industry has impressed end users by delivering new functionality every two years. The main platform for delivering new functionality was transistor scaling, aka Moore's law. Today, 3D technology is emerging as the next paradigm beyond Moore's law, as it is the platform for heterogeneous integration. In this talk, we will therefore outline the status of 3D technology, and indicate how it will revolutionize the semiconductor industry over the upcoming decades.
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